REMARKS

Applicants thank the Examiner for the total consideration given the present application. Claims 1-6 remain pending. Applicants appreciate that the previously issued Election/Restriction requirement has been withdrawn. Claims 5 and 6 have been amended through this Reply. Claims 1-6 are independent. Favorable reconsideration and allowance of the present application are respectfully requested in view of the following remarks.

ALLOWABLE SUBJECT MATTER

Applicants appreciate that claims 1-4 are indicated as allowable.

PRIOR ART REJECTION

Claims 5 and 6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by ***Schiefer et al.*** (U.S. Patent 6,177,922). Applicants respectfully traverse this rejection.

As amended, independent claim 5 now recites an apparatus, which includes the ***clock signal that is asynchronous to the input horizontal synchronization signal***. The image conversion module configured to ***receive the control signal for arbitrarily setting a conversion ratio for an input image and*** to generate an output image signal ***at the arbitrary conversion ratio*** based on an input image signal, the output vertical and horizontal synchronization signals, and the ***cycle information*** of the clock signal ***that is asynchronous to the input horizontal synchronization signal***.

As previously submitted, in conventional image display devices, arbitrary conversion ratios cannot be set, so only conversion images smaller or greater than the display area size of the display panel can be generated. Applicants respectfully submit that the present invention as claimed, *inter alia*, has solved the problem of conventional image display devices as mentioned above. Specifically, control signal is utilized to arbitrarily set a conversion ratio for the input image and the cycle information of the clock signal that is asynchronous to the input horizontal synchronization signal is utilized as part of the control signal to generate the output image signal.

Schiefer discloses a conventional format converter 110 which is capable of accepting as input a digital video input signal (i.e., an input horizontal synchronization signal (IPHSYNC))

that has a first viewable display resolution, pixel rate, and line rate, and producing as output a second digital video signal that has a different display resolution, pixel rate, and line rate. As shown in FIG. 3, the format converter 110 includes a memory write controller 300, memory 310, a display processor 320, and a display timing controller 330. This format converter 110 achieves the conversion from the input format to the display output format by processing input lines of pixel data using a de-interlacing, filtering, and scaling algorithm to generate a desired display output format. Further, Schiefer discloses that the memory 310 is provided in the format converter data path in order to accommodate a video input clock (IPCLK) that can be running ***asynchronous*** to the display output clock (DCLK). (*See col. 9, lines 8-26.*)

Schiefer is distinguished from the claimed invention in that Schiefer fails to teach or suggest "an image conversion module configured to ***receive the control signal for arbitrarily setting a conversion ratio for an input image*** and to generate an output image signal ***at the arbitrary conversion ratio*** based on an input image signal, the output vertical and horizontal synchronization signals, and the ***cycle information*** of the ***clock signal that is asynchronous to the input horizontal synchronization signal***." Although Schiefer discloses that the video IPCLK may run asynchronous to the DCLK, Schiefer provides no indication that a control signal is generated for arbitrarily setting a conversion ratio for an input image and to generate an output image signal at the arbitrary conversion ratio based on at least a clock signal that is asynchronous to the IPHSYNC.

Therefore, for at least the above reasons, it is respectfully submitted that claim 5 is allowable over Schiefer. Claim 6 is directed to a method corresponding to claim 5 which recites, *inter alia*, "***outputting the control signal for arbitrarily setting a conversion ratio for an input image***; and generating an output image signal ***at the arbitrary conversion ratio*** based on an input image signal, the output vertical and horizontal synchronization signals, and ***cycle information*** of ***the clock signal that is asynchronous to the input horizontal synchronization signal***. Thus, it respectfully submitted that claim 6 is also allowable over Schiefer for at least the reasons set forth above with respect to claim 5.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Ali M. Imam Reg. No. 58,755 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

By Ali Imam #58,755

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